BPPSA: Scaling Back-propagation by Parallel Scan Algorithm

by

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A thesis submitted in conformity with the requirements
for the degree of Master of Science
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Abstract

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2020

In an era when the performance of a single compute device plateaus, software must be designed to scale on a massively parallel system for better runtime performance. However, in the context of training deep learning models, the commonly used back-propagation (BP) algorithm imposes a strong sequential dependency in the process of gradient computation. Under model parallelism, BP has a theoretical step complexity of $\Theta(n)$ which hinders its scalability in a parallel computing environment, where $n$ represents the number of compute devices into which a model is partitioned.

Scan is a primitive operation that performs an in-order aggregation on a sequence of values and returns the partial result at each step. Parallel algorithms (e.g., Blelloch scan) have been developed to scale the scan operation on massively parallel systems. In this work, in order to improve the scalability of BP, we reformulate BP into a scan operation which is then scaled by our modified version of the Blelloch scan algorithm with a theoretical step complexity of $\Theta(\log n)$. We evaluate our approach on a vanilla Recurrent Neural Network (RNN) training with synthetic datasets, and demonstrate up to $2.75 \times$ speedup in terms of the overall training time and $8.8 \times$ speedup on the backward pass alone; we also evaluate on a RNN with Gated Recurrent Units (GRU) training with the IRMAS dataset, and demonstrate up to $2.11 \times$ speedup in terms of the overall training time and $13.45 \times$ speedup on the backward pass runtime.
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Chapter 1

Introduction

The training of deep learning models demands more and more compute resources as the models become more powerful and complex with an increasing number of layers in recent years [35, 59, 58, 25, 29]. For example, ResNet can have more than a thousand layers [26], and ResNet-152 takes days to train on eight state-of-the-art GPUs [17]. Now that the performance of a single compute device plateaus [20], training has to be designed to scale on a massively parallel system.

Data parallelism [57] is the most popular way to scale training by partitioning the training data among multiple devices, where each device contains a full replica of the model. As the number of devices increases, data parallelism faces the trade-off between the synchronization cost in synchronous parameter updates and staleness in asynchronous parameter updates [6]. Moreover, data parallelism cannot be applied when a model does not fit into one device due to memory constraints (e.g., caused by deep network architecture, large batch size, or high input resolution [53, 63]).

Model parallelism [34, 30, 43] is another approach to distributed training which partitions a model and distributes its parts among devices. It covers a wide spectrum of training deep learning models where data parallelism does not suffice. Naïve training under model parallelism does not scale well with the number of devices due to under-utilization of the hardware resources, since at most one device can be utilized at any given point in time [43]. To address the aforementioned issue, prior works on pipeline parallelism, including PipeDream [43] and GPipe [30], propose pipelining across devices for better resource utilization; however, as the number of layers and devices increases, pipeline parallelism still faces the trade-off between the resource utilization in synchronous parameter updates and staleness in asynchronous parameter updates [43]. Moreover, to fully fill the pipeline with useful computation, each device needs to store the activations at the partition boundaries of all mini-batches that enters the pipeline. Therefore, the maximum number of devices that pipeline parallelism can support is limited by the memory capacity of a single device.

Algorithmically, the fundamental reason for this scalability limitation observed from prior works is that the back-propagation (BP) algorithm [54] imposes a strong sequential dependency between layers during the gradient computation. Since computing systems evolve to have more and more parallel nodes [20], in this work, we aim at exploring the following question: How can BP scale efficiently when the number of layers and devices keeps increasing in the foreseeable future?

To answer this question, we utilize a primitive operation called Scan [10] that performs an in-order aggregation on a sequence of values and returns the partial result at each step. Parallel algorithms [28, 10]
have been developed to scale the scan operation on massively parallel systems. We observe that BP is mathematically similar to a scan operation on the transposed Jacobian matrix \[62\] of each layer and the gradient vector of the output from the last layer. Inspired by this key observation, we restructure the strong sequential dependency of BP, and present a new method to scale Back-propagation by Parallel Scan Algorithm (BPPSA). Our major contributions are summarized below.

We reformulate BP as a scan operation and modify the Blelloch scan algorithm \[10\] to efficiently scale BP in a distributed computing environment. Our method has a theoretical step complexity of \(\Theta(\log n)\), where \(n\) represents the number of devices into which a model is partitioned, compared to \(\Theta(n)\) of the naïve implementation of model parallelism. Moreover, our algorithm does not have the theoretical scalability limits by the memory capacity of a single device as pipeline parallelism does. As an example, Figure 1.1 shows how BP for training a network composed of 7 layers (blue cubes) can be reformulated into a scan operation on the transposed Jacobian matrices (blue squares) of this network and the final gradient vector (yellow squares), as well as how this scan operation can be scaled by BPPSA.

Generating, storing and processing full Jacobian matrices are usually considered to be prohibitively expensive. However, we observe that the Jacobian of many layers can be extremely sparse where traditionally we can leverage sparse matrix format \[55\] to reduce the runtime and storage costs; more importantly, the positions of input-independent zeros in the Jacobian are deterministic, which leads to potentially more optimized implementations of sparse matrix libraries. Based on these observations, we develop routines to efficiently generate sparse transposed Jacobian for various operators.

As a proof of concept, we evaluate BPPSA on a vanilla Recurrent Neural Network (RNN) \[19\] training with synthetic datasets, and achieve a maximum 2.75× speedup in terms of the overall (end-to-end) training time and a 8.8× speedup on the backward pass, compared to the baseline BP approach which under-utilizes the GPU. We also evaluate BPPSA on a RNN with Gated Recurrent Units (GRU) \[16\] training with the IRMAS dataset \[11\] for the task of instrument classification from audio signals, and achieve a maximum 2.11× overall speedup and a 13.45× speedup on the backward pass. Moreover, we demonstrate that the retraining of pruned networks \[24, 56, 27\] can also be a practical use case of BPPSA.

---

1Step complexity (detailed in Section 3.6) quantifies the runtime of a parallel algorithm.
Chapter 2

Background and Motivation

2.1 Problem Formulation

We conceptualize a deep learning model as a vector function \( f \) composed of sub-functions \( \vec{x}_i = f_i(\vec{x}_{i-1}; \vec{\theta}_i) \):

\[
\begin{align*}
\vec{f} \coloneqq (\vec{f}_1(\vec{x}_0; \vec{\theta}_1), \ldots, \vec{f}_n(\vec{x}_n; \vec{\theta}_n)) = \vec{f}_1(\vec{x}_0; \vec{\theta}_1) \odot \ldots \odot \vec{f}_n(\vec{x}_n; \vec{\theta}_n)
\end{align*}
\] (2.1)

where \( \vec{\theta}_i, i \in \{1, \ldots, n\} \) are the parameters of the model. The model is evaluated by an objective function \( l(f(\vec{x}_0; \vec{\theta}_i, i \in \{1, \ldots, n\})) \), where \( \vec{x}_0 \) is the initial input to the model. Figure 2.1 visualizes a convolutional neural network conceptualized in this formulation.

To train the model \( f \), a first-order optimizer requires the gradients \( \nabla \vec{\theta} l \), which are derived from the gradients \( \nabla \vec{x} l \):

\[
[\nabla \vec{\theta}_1 l, \ldots, \nabla \vec{\theta}_n l] \leftarrow [(\frac{\partial \vec{x}_1}{\partial \vec{\theta}_1})^T \nabla \vec{x}_1 l, \ldots, (\frac{\partial \vec{x}_n}{\partial \vec{\theta}_n})^T \nabla \vec{x}_n l]
\] (2.2)

where \( \frac{\partial \vec{x}_i}{\partial \vec{\theta}_i} \) is the Jacobian matrix of the output \( \vec{x}_i \) of \( f_i \) to its parameters \( \vec{\theta}_i \). To derive \( \nabla \vec{x} l \) given \( \nabla \vec{x}_n l \), BP [54] solves the following recursive equation, from \( i = n - 1 \) to \( i = 1 \):

\[
\nabla \vec{x}_i l \leftarrow (\frac{\partial \vec{x}_{i+1}}{\partial \vec{x}_i})^T \nabla \vec{x}_{i+1} l, \forall i \in \{n - 1, \ldots, 1\}
\] (2.3)

where \( \frac{\partial \vec{x}_{i+1}}{\partial \vec{x}_i} \) is the Jacobian matrix of the output \( \vec{x}_{i+1} \) of \( f_{i+1} \) to its input \( \vec{x}_i \). Equation 2.2 itself does not have dependency along \( i \); therefore, the computation of \( \nabla \vec{x}_i l \) can be parallelized if \( \nabla \vec{x}_i l \) are available. However, Equation 2.3 imposes a strong sequential dependency along \( i \) where the computation of \( \nabla \vec{x}_i l \) cannot begin until the computation of \( \nabla \vec{x}_{i+1} l \) finishes, and therefore, hinders the scalability when multiple workers (as an abstraction of devices) are available.

2.2 Prior Works

To increase the utilization of hardware resources in model parallelism, prior works, e.g., PipeDream [43] and GPipe [30], propose to pipeline the computation in the forward and backward passes across devices. However, these solutions are not “silver bullets” to scalability due to the following reasons.

First, both PipeDream [43] and GPipe [30] require storing activations and/or multiple versions of
weights for all batches that enter the pipeline. Although GPipe’s re-materialization [14] can mitigate the memory usage, the theoretical space complexity still grows linearly with the length of the pipeline (i.e., the number of devices). As a result, the maximum number of devices that pipeline parallelism can support is limited by the memory capacity of a single device (e.g., the GPU global memory), and such memory capacity is not expected to grow significantly in a foreseeable future [41].

**Space Complexity of GPipe** Using the notations consistent with GPipe, with re-materialization enabled, each device reserves \( \Theta(L/K) \) space for re-computing the intermediate activations of each sample in a “micro-batch”, where \( L \) and \( K \) are the length of the network and the number of devices in the pipeline correspondingly. As we show in Figure 2.2 to fully fill the pipeline with useful computation, the number of “micro-batches” entering the pipeline (the solid black box) should be equal to the length of the pipeline (the dashed black box); thus, each device needs to store at least \( \Theta(K) \) activations at the partition boundary for each sample, resulting in a \( \Theta(L/K + K) \) per-device space complexity.

Second, if the parameter updates are partially asynchronous, as proposed in PipeDream [43], staleness will be introduced. Although Narayanan et al. argue that the staleness produced by their method does not affect the update step for a vanilla SGD optimizer [43], such an argument would be invalid when combined with other techniques commonly used in first-order optimizers (e.g., momentum in Adam [32]). If, however, the gradient updates are fully synchronized as proposed in GPipe [30], the “bubble of idleness” between the forward and backward passes increases linearly with the length of the pipeline, thus, linearly reducing the hardware utilization and decimating the original purpose of pipelining.
Our approach fundamentally differs from these key prior works [43, 30] in the following major ways. First, instead of following the dependency of BP, we reformulate BP so that scaling is achieved via the Blelloch scan algorithm [10] which is designed for parallelism. Second, the original BP is reconstructed exactly without introducing new sources of errors (e.g., staleness); therefore, our method is agnostic to the exact first-order optimizer being used. Third, our approach becomes more advantageous as the number of devices increases, instead of diminishing returns or hitting scalability limits due to linear per-device space complexity.

2.3 Definition of the Scan Operation

For a binary and associative operator ⊕ with an identity value $I$, the exclusive scan (a.k.a., prescan) on an input array $[a_0, a_1, a_2, ..., a_{n-1}]$ produces an output array $[I, a_0, a_0 ⊕ a_1, a_0 ⊕ a_1 ⊕ a_2, ..., a_0 ⊕ ... ⊕ a_{n-2}]$ [10]. Parallel scan algorithms were developed as both the importance of the scan operation and the parallelism of the hardware and systems increase [28, 10].
Chapter 3

Proposed Method: BPPSA

3.1 Back-propagation as a Scan Operation

We define a binary, associative, and non-commutative operator $A \circ B = BA$, whose identity value is the identity matrix $I$, where $A$ can be either a matrix or a vector and $B$ is a matrix. Using operator $\circ$, we can reformulate Equation 2.3 as calculation of the following array:

$$\begin{bmatrix}
\nabla \vec{x}_n, \nabla \vec{x}_n \circ (\frac{\partial \vec{x}_n}{\partial \vec{x}_{n-1}})^T, \nabla \vec{x}_n \circ (\frac{\partial \vec{x}_{n-1}}{\partial \vec{x}_{n-2}})^T, ..., \nabla \vec{x}_n \circ (\frac{\partial \vec{x}_n}{\partial \vec{x}_1})^T \circ ... \circ (\frac{\partial \vec{x}_2}{\partial \vec{x}_1})^T
\end{bmatrix}$$  \hspace{1cm} (3.1)

Equation 3.1 can be interpreted as an exclusive scan operation of $\circ$ on the input array:

$$\begin{bmatrix}
\nabla \vec{x}_n, (\frac{\partial \vec{x}_n}{\partial \vec{x}_{n-1}})^T, (\frac{\partial \vec{x}_{n-1}}{\partial \vec{x}_{n-2}})^T, ..., (\frac{\partial \vec{x}_2}{\partial \vec{x}_1})^T, (\frac{\partial \vec{x}_1}{\partial \vec{x}_0})^T
\end{bmatrix}$$  \hspace{1cm} (3.2)

3.2 Scaling Back-propagation with the Blelloch Scan Algorithm

We parallelize the computation of Equation 3.1 on multiple workers with the Blelloch scan algorithm \[10\], formally described in Algorithm 1. The algorithm contains two phases: up-sweep and down-sweep. As an example, Figure 3.1 visualizes this algorithm applied on the convolution layers of VGG-11 \[58\] with levels L0-L4 as the up-sweep and levels L5-L10 as the down-sweep. Only the up-sweep phase contains matrix-matrix multiplications. Due to the non-commutative property of the operator $\circ$, we have to reverse the order of operands for $\circ$ during the down-sweep phase. This modification is reflected on line 13 of Algorithm 1 and visualized in Figure 3.2b.

3.3 Jacobian Matrices in Sparse Format

A full Jacobian matrix $\frac{\partial \vec{x}_{i+1}}{\partial \vec{x}_i}$ of $f_{i+1}(\cdot; \vec{\theta}_{i+1})$ can be too expensive to generate, store, and process. In fact, the Jacobian matrix of the first convolution operator in VGG-11 \[58\] processing a $32 \times 32$ image can occupy 768 MB of memory if it is stored as a full matrix, which is prohibitively large. Fortunately, Jacobian matrices of major operators (such as convolution, ReLU, and max-pooling) are usually extremely sparse as shown in Figure 3.3. In comparison, representing the data contained in the same Jacobian of the aforementioned convolution operator in the Compressed Sparse Row (CSR) \[55\] format shrinks
Figure 3.1: Applying our algorithm on the convolution layers of VGG-11 [58]. Blue, orange, and green squares represent transposed Jacobian matrices, gradient vectors, and \textit{symbolic} identity matrices respectively. Blue solid lines, orange solid lines, and yellow dash lines represent matrix-matrix multiplications, matrix-vector multiplications, and \textit{logical} data movements (that do not have to be performed explicitly) respectively.

(a) Up-sweep: $B \leftarrow A \odot B$.

(b) Down-sweep: $A, B \leftarrow B, B \odot A$.

Figure 3.2: Visualizations of the primitive operations performed in the up-sweep and the down-sweep phases.

the memory consumption down to only 6.5 MB. We can observe that there are two reasons for zeros to appear in an operator’s Jacobian: \textit{guaranteed zeros} that are input ($\mathbf{x}_0$) invariant (e.g., zeros that are not on the diagonal of the ReLU’s Jacobian) and related to the model’s architecture; and \textit{possible zeros} that depend on the input (e.g., zeros on the diagonal of the ReLU’s Jacobian). For any operator, the positions of guaranteed zeros (named as the \textit{sparsity pattern} for brevity) in the Jacobian is \textit{deterministic} with the model architecture and known \textit{ahead of time}. Thus, mapping non-zero elements in the input matrices to each non-zero element in the product matrix (e.g., calculating the number of non-zeros and index merging in CSR matrix-matrix multiplication [37]) can be performed prior to training and removed from a generic sparse matrix multiplication routine (e.g., cuSPARSE [45]) to achieve significantly better performance during the training phase. The sparsity of guaranteed zeros (defined as the fraction over all elements in a matrix) for various operators is listed in Table 3.1. In our implementation, the transposed Jacobian matrices are represented in the CSR format since it is the most straightforward and commonly used sparse matrix format; however, any other sparse matrix format can be used as an alternative, including a potentially more efficient customized sparse matrix format that utilizes the deterministic property of the current sparsity pattern.
Algorithm 1 Modified Blelloch Scan Algorithm

Input: $a = [\nabla_{x_i} I, \frac{\partial \nabla_{x_i} I}{\partial x_{n-1}}, ..., \frac{\partial \nabla_{x_i} I}{\partial x_0}]$  \hspace{1cm} $\triangleright$ Input array of Equation 3.2
Output: $a = [I, \nabla_{x_i} l, ..., \nabla_{x_i} l]$  \hspace{1cm} $\triangleright$ $\nabla_{x_i} l$ for Equation 2.2 computed in-place

1. for $d \leftarrow 0$ to $\lceil \log(n+1) \rceil - 2$ do
2.   for all $i \leftarrow 0$ to $(n - 2^d)$ by $2^{d+1}$ do in parallel
3.     $(l, r) \leftarrow (i + 2^d - 1, \min(i + 2^{d+1} - 1, n))$
4.     $a[r] \leftarrow a[l] \odot a[r]$
5. end for
6. end for
7. $a[n] \leftarrow I$
8. for $d \leftarrow \lceil \log(n+1) \rceil - 1$ to 0 do
9.   for all $i \leftarrow 0$ to $(n - 2^d)$ by $2^{d+1}$ do in parallel
10.  $(l, r) \leftarrow (i + 2^d - 1, \min(i + 2^{d+1} - 1, n))$
11.  $T \leftarrow a[l]$
12.  $a[l] \leftarrow a[r]$
13.  $a[r] \leftarrow a[r] \odot T$
14. end for
15. end for

$\triangleright$ Modification: Reverse the operands of $\odot$.

Table 3.1: The sparsity of guaranteed zeros for various operators.

<table>
<thead>
<tr>
<th>Operator</th>
<th>Filter/Kernel Size</th>
<th>Input Size</th>
<th>Output Size</th>
<th>Sparsity</th>
<th>Examples $\uparrow$</th>
<th>Analytical Generation Speedup $\downarrow$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Convolution</td>
<td>$c_0 \times c_i \times h_f \times w_f$</td>
<td>$c_i \times h_i \times w_i$</td>
<td>$c_0 \times h_o \times w_o$</td>
<td>$1 - \frac{h_f w_f}{h_i w_i}$</td>
<td>0.99157</td>
<td>$8.3 \times 10^3 \times$</td>
</tr>
<tr>
<td>ReLU</td>
<td>N/A</td>
<td>$c \times h \times w$</td>
<td>$c \times h \times w$</td>
<td>$1 - \frac{1}{c h w}$</td>
<td>0.99998</td>
<td>$1.2 \times 10^6 \times$</td>
</tr>
<tr>
<td>Max-pooling</td>
<td>$h_f \times w_f$</td>
<td>$c_i \times h_i \times w_i$</td>
<td>$c_0 \times h_o \times w_o$</td>
<td>$1 - \frac{h_f w_f}{c_i h_i w_i}$</td>
<td>0.99994</td>
<td>$1.5 \times 10^5 \times$</td>
</tr>
</tbody>
</table>

$\uparrow$ The examples of sparsity for the first convolution, ReLU and max-pooling operators of VGG-11 [58] operating on $32 \times 32$ images are shown in the second last column of the table.
$\downarrow$ Approximation when $h_i$ and $w_i$ are much greater than the padding size.
$\odot$ Over generating the transposed Jacobian through PyTorch’s Autograd [49] one column at a time; measured on a Ryzen Threadripper 1950X [2] machine; averaged across 1000 trials.

3.4 Generating Jacobian Matrix in CSR Analytically

To practically generate the Jacobian for an operator, instead of generating one column at a time either numerically [49] or via automatic differentiation [49] [50], we develop analytical routines to generate the transposed Jacobian directly into the CSR format. For example, Algorithm 2, Algorithm 3 and Algorithm 4 show how to generate the CSR indptr, indices and data arrays [61] respectively for the transposed Jacobian of a convolution operator that has a $3 \times 3$ filter and padding size of 1. The last column of Table 3.1 shows the speedup on analytical generation of the transposed Jacobian for different operators in VGG-11 [58]. To build a mature framework with automatic differentiation capability that performs training via our method, one would need to build an equivalent of the cuDNN library [49] which possesses a “sparse transposed Jacobian operator” in place of a backward operator for each forward operator.

$^1$ Although the example uses a specific configuration of the convolution operator, deriving a generic routine is doable.
**Algorithm 2** Compute the CSR `indptr` array for the transposed Jacobian of a $3 \times 3$ convolution.

**Input:** input channels $c_i$, output channels $c_o$, input height $h_i$, input width $w_i$  
**Output:** `indptr` ← malloc($c_ih_iw_i + 1$)

1. for all $i \leftarrow 0$ to $(c_ih_iw_i)$ do in parallel  
2. $a \leftarrow \lfloor i/(h_iw_i) \rfloor$  
3. $b \leftarrow i \bmod (h_iw_i)$  
4. if $b \leq w_i$ then  
5. \hspace{1em} `indptr[i]` $\leftarrow ac_o(3w_i(3h_i - 2)) + 6c_ob$  
6. else if $b \leq w_i(h_i - 1)$ then  
7. \hspace{1em} `indptr[i]` $\leftarrow ac_o(3w_i(3h_i - 2)) + 6c_ow_i + 9c_o(b - w_i)$  
8. else  
9. \hspace{1em} `indptr[i]` $\leftarrow ac_o(3w_i(3h_i - 2)) + 6c_ow_i + 9c_o(w_i(h_i - 2)) + 6c_o(b - w_i(h_i - 1))$  
10. end if  
11. end for

**Algorithm 3** Compute the CSR `indices` array for the transposed Jacobian of a $3 \times 3$ convolution.

**Input:** input channels $c_i$, output channels $c_o$, input height $h_i$, input width $w_i$, `indptr` computed from Algorithm 2  
**Output:** `indices` ← malloc($3w_i(3h_i - 2)c_ic_o$)

1. for all $i \leftarrow 0$ to $(c_ih_iw_i - 1)$ do in parallel  
2. $r \leftarrow i \bmod (h_iw_i)$  
3. `base` ← malloc($9c_o$)  
4. for all $j \leftarrow 0$ to $(c_o - 1)$ do in parallel  
5. \hspace{1em} for all $k \leftarrow 0$ to $2$ do in parallel  
6. \hspace{2em} `base[9j + 3k : 9j + 3(k + 1)]` $\leftarrow ([-1, 0, 1] + (jh_i + k - 1)w_i + r) \bmod (c_o h_i w_i)$  
7. \hspace{1em} end for  
8. end for  
9. if $r < w_i$ or $r \geq w_i(h_i - 1)$ then  
10. \hspace{1em} `row` ← malloc($6c_o$)  
11. \hspace{1em} `(left, right)` $\leftarrow (3, 9)$ if $r < w_i$; $(0, 6)$ otherwise  
12. \hspace{1em} for all $j \leftarrow 0$ to $(c_o - 1)$ do in parallel  
13. \hspace{2em} `row[6j : 6j + 6]` $\leftarrow `base[9j + left : 9j + right]$  
14. \hspace{1em} end for  
15. else  
16. \hspace{1em} `row` $\leftarrow `base$  
17. end if  
18. `indices[indptr[i] : indptr[i + 1]]` $\leftarrow `sorted(row)$  
19. end for
Algorithm 4 Compute the CSR data array for the transposed Jacobian of a $3 \times 3$ convolution.

**Input:** input channels $c_i$, output channels $c_o$, input height $h_i$, input width $w_i$, filter weights, indptr computed from Algorithm 2

**Output:** data $\leftarrow$ malloc($3w_i(3h_i - 2)c_ic_o$)

1. for all $i \leftarrow 0$ to $(c_i h_i w_i - 1)$ do in parallel
2. $r \leftarrow i \mod (h_i w_i)$
3. $m \leftarrow \lfloor i/(h_i w_i) \rfloor$
4. range $\leftarrow (1: -1)$ if ($r < w_i$); $(2: 0: -1)$ if ($r \geq w_i(h_i - 1)$); $(2: : -1)$ otherwise
5. data[indptr[i] : indptr[i + 1]] $\leftarrow$ flatten(weights[ :, m, range, :: -1])
6. Fix corner cases when ($i \mod w_i = 0$ or ($i \mod w_i = (w_i - 1)$).

3.5 Convergence

Theoretically, our algorithm is a reconstruction of BP instead of an approximation, and hence, expected to reproduce the exact same outputs. However, in practice, numerical differences could be introduced due to the change in the order of matrix multiplications. We apply our algorithm to train LeNet-5 [38] on CIFAR-10 [33] to demonstrate that such numerical differences would not affect model convergence. We use a mini-batch size of 256 and the SGD [32] optimizer with a learning rate of 0.001 and a momentum of 0.9. The experiments are seeded with the same constant. Figure 3.4 shows that the orange lines overlap.
Figure 3.4: Training and test loss per iteration for training LeNet-5 on CIFAR-10. The orange solid lines represent training via the PyTorch Autograd baseline, while the blue dash lines represent training via BPPSA.

with the blue lines for both training and test losses, which means our algorithm has negligible impact on the convergence compared to the original BP.

3.6 Complexity Analysis

Runtime Complexity  We leverage the following definitions to quantify the complexity of a parallel algorithm: (1) step complexity ($S$) which evaluates the minimum number of steps to finish the execution on the critical path (end-to-end) given the number of parallel workers; (2) per-step complexity ($P$) which evaluates the runtime of a single step; and (3) work complexity ($W$) which evaluates the number of total steps executed by all workers. For brevity, we refer to performing the scan operation serially as linear scan, which is essentially emulating BP by using the transposed Jacobian and multiplying it with the gradient (as shown in Equation 2.3) explicitly. Assuming the system can be conceptualized as a parallel random-access machine (PRAM), the number of workers is $p$ and the size of the input array in Equation 3.2 is $n + 1$, the step and work complexity of our algorithm can be derived as:

$$S_{\text{Blelloch}}(n) = \begin{cases} \Theta(\log n) & p > n \\ \Theta(n/p + \log p) & \text{otherwise} \end{cases}$$

(3.3)

$$W_{\text{Blelloch}}(n) = \Theta(n)$$

(3.4)

compared to $S_{\text{Linear}}(n) = \Theta(n), W_{\text{Linear}}(n) = \Theta(n)$ of the linear scan (which has the same step and work complexity as BP). Therefore, in an ideal scenario where there is an unbounded number of workers with unit per-step complexity, our algorithm reduces the runtime of BP from $\Theta(n)$ to $\Theta(\log n)$. If, however, we consider the difference in per-step complexity between our algorithm ($P_{\text{Blelloch}}$) and the baseline ($P_{\text{Linear}}$) due to runtime difference between matrix-matrix and matrix-vector multiplications,

\footnote{We can derive the same conclusion from Figure 5.1 and Figure 5.3}
Chapter 3. Proposed Method: BPPSA

our algorithm has a runtime of $\Theta(\log n) P_{Blelloch}$ compared to $\Theta(n) P_{Linear}$ in the baseline. There are two approaches to make our algorithm achieve a lower runtime and better scaling than the baseline. First, we can reduce $P_{Blelloch}$, which is reflected in leveraging the sparsity in the transposed Jacobian as analyzed in Section 4.3 and Section 5.3. Second, without a lower $P_{Blelloch}$, our algorithm can still outperform the baseline if $P_{Blelloch}/P_{Linear} < \Theta(n/\log n)$. This can occur when $n/\log n$ grows larger than the dimension of $\bar{x}_i$. The performance benefit of such case is demonstrated in Section 4.1, Section 4.2, Section 5.1 and Section 5.2.

**Space Complexity**  
Assuming space of storing a transposed Jacobian matrix is bounded by $M_{Jacob}$ and storing $\bar{x}_i$ is bounded by $M_{\bar{x}}$ (note that $M_{Jacob} \ll O(M_{\bar{x}}^2)$ due to sparse matrix formats; both $M_{Jacob}$ and $M_{\bar{x}}$ are not functions of $p$), in our method, each worker requires the space of $M_{Blelloch}(n) = \Theta(max(\frac{n}{p}, 1)) M_{Jacob}$ which reduces as $p$ increases until a constant $M_{Jacob}$, comparing to $M_{pipeline} = \Theta(\frac{n}{p} + p) M_{\bar{x}}$ of pipeline parallelism which increases linearly as $p$ increases. Therefore, our method does not have the limitation of scalability on $p$, as long as each worker has the memory capacity of at least $M_{Jacob}$. 
Chapter 4

Methodology

Although there have been many prior works in the industry of training deep learning models on thousands of devices [40] which result in $p$ being on the similar scale of $n$, setting up an experiment for such a high number of devices would require a data center of GPUs and re-implementing/optimizing our entire experiment framework, which requires both monetary and engineering resources out of reach for a typical academic research group. Therefore, we setup a set of small-scale experiments that can reflect the large-scale workloads to demonstrate the potential performance benefits of our method.

**Environment Setup**  Our experiments are performed on two platforms with RTX 2070 [47] and RTX 2080Ti [48] respectively (both are Turing architecture GPUs) whose specifications are listed in Table 4.1.

<table>
<thead>
<tr>
<th>Table 4.1: Specifications of our experiment platforms.</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>GPU</strong></td>
</tr>
<tr>
<td>Number of Streaming Multiprocessors (SMs)</td>
</tr>
<tr>
<td>CUDA [44]</td>
</tr>
<tr>
<td>cuDNN [45]</td>
</tr>
<tr>
<td>PyTorch [49]</td>
</tr>
<tr>
<td>CPU</td>
</tr>
<tr>
<td>Host Memory</td>
</tr>
<tr>
<td>Linux Kernel [60]</td>
</tr>
</tbody>
</table>

**Baselines**  We evaluate our method against *PyTorch Autograd* [49] with cuDNN backend [46] which is a widely adopted and state-of-the-art implementation of BP. [41]

**Metrics**  We use three metrics to quantify the results from our evaluations: 1) *wall-clock time* which measures the system-wide actual time spent on a process, 2) *speedup* which is the ratio of the wall-clock time spent on the baseline over our method, and 3) *FLOP* which represents the number of floating-point operations executed.

We leverage three types of benchmarks to empirically evaluate BPPSA: (1) an end-to-end benchmark of a vanilla RNN training on synthesized datasets to demonstrate the scalability benefits of BPPSA on

---

1We also attempted to prototype a pipeline parallelism implementation via CUDA streams in our experiments; however, such implementation incurs significant overhead, thus performs much worse than our baseline.
long sequential dependency; (2) an end-to-end benchmark of a GRU training on the IRMAS dataset to demonstrate the potentials of BPPSA on a more realistic workload; and (3) a micro-benchmark of a pruned VGG-11 to evaluate the feasibility of using sparse matrix format to reduce the per-step complexity of BPPSA.

### 4.1 RNN End-to-end Benchmark with Synthetic Datasets

We setup experiments of training a RNN on sequential data, which is a classical example of workloads where the runtime performance (in terms of the wall-clock time) is limited due to the strong sequential dependency. The large number of operators \( n \) is modeled through a large sequence length \( T \), and the large number of workers \( p \) is reflected in the total number of CUDA threads that can be executed concurrently in all SMs of a single GPU normalized by the mini-batch size \( B \).

#### Datasets
We synthesize the datasets \( X = \{(x^{(k)}, c^{(k)})\} \) of 32000 training samples (i.e., \( k \in \{0, 31999\} \)) for the task of bitstream classification. Each sample consists of a class label \( c^{(k)} \) where \( c^{(k)} \in \{0, \ldots, 9\} \) and a bitstream \( x^{(k)} \) where the value \( x_t^{(k)} \) at each time step \( t \in \{0, \ldots, T-1\} \) is sampled from the Bernoulli distribution:

\[
x_t^{(k)} \sim \text{Bernoulli}(0.05 + c^{(k)} \times 0.1)
\]

Equivalently, each bitstream \( x^{(k)} \) can be viewed as a binomial experiment of class \( c^{(k)} \). A set of examples is visualized in Figure 4.1. The objective of this task is to classify each bitstream \( x^{(k)} \) into its corresponding class \( c^{(k)} \) correctly. We synthesize eight datasets with different \( T \), where \( T \) increases up to 30000. In reality, long sequences of input can often be found in audio signals such as speech or music.

![Figure 4.1: Examples of bitstreams in the bitstream classification task when the sequence length \( T = 10 \). The expectation of the number of ones in the bitstream \( x^{(k)} \) is \( T \times (0.05 + c^{(k)} \times 0.1) \).](image)

#### Model
We leverage a vanilla RNN (described in Equation 4.2) to solve the aforementioned task since RNN is an intuitive, yet classical, deep learning model and often used to process sequential data:

\[
\tilde{h}_t^{(k)} = \tanh(W_{ih} x_t^{(k)} + \vec{b}_{ih} + W_{hh} \tilde{h}_{t-1}^{(k)} + \vec{b}_{hh})
\]
where $\vec{h}_t^{(k)}, \vec{b}_{hh}, \vec{b}_{hh} \in \mathbb{R}^{20}$. The output classes are predicted via the softmax function applied on a linear transformation to the last hidden states $\vec{h}_{T-1}^{(k)}$. The cross entropy is used as the loss function which is optimized in training via the Adam optimizer with the learning rate of $3 \times 10^{-5}$. The computation of $\nabla_{\vec{h}_t^{(k)}} l$ during the backward pass carries the strong sequential dependency which is the target for acceleration via BPPSA.

**Implementation** Our modified version of the Blelloch scan algorithm is implemented as two custom CUDA kernels for the up-sweep and down-sweep phases respectively, along with a few other CUDA kernels for the preparation of the input transposed Jacobian matrices. Each level during the up-/down-sweep phase requires a single CUDA kernel launch, therefore synchronization is ensured between two consecutive levels. Each thread block is responsible for the operation (i.e. multiplication in reverse) of two matrices as well as moving the intermediate results, and the shared memory is leveraged for caching input and output matrices. Our custom CUDA kernels are integrated into the Python front-end where the RNN and the training procedure are defined through PyTorch’s Custom C++ and CUDA Extensions. For the forward pass and the baseline of PyTorch Autograd, we are using the PyTorch’s RNN module directly which calls into the cuDNN’s RNN implementations (cudnnRNNForwardTraining and cudnnRNNBackwardData), therefore, our baseline is already much faster than implementing RNN in Python using PyTorch’s RNNCell module due to GEMM streaming and operation fusions.

### 4.2 GRU End-to-end Benchmark with IRMAS

To extend the aforementioned RNN end-to-end benchmark to a more realistic workload, we evaluate the runtime performance of training a GRU on the IRMAS dataset for the task of instrument classification.

**Datasets** We preprocess the IRMAS dataset and compute the mel-frequency cepstral coefficients (MFCC) for each waveform audio sample via the MFCC implementation provided by LibROSA. With different MFCC configurations as listed in Table 4.2, the preprocessing results in three sets (S, M, and L) reflecting the trade-off between the temporal and frequency resolutions. For all samples, the values of each coefficient along the frames are normalized to have zero mean and unit variance. We ignore and remove the first coefficient because it only represents the average power of the audio signal.

Table 4.2: MFCC configurations and resulting feature size (frames $\times$ coefficients) for the S, M and L sets.

<table>
<thead>
<tr>
<th>Set Name</th>
<th>MFCC Coefficients</th>
<th>FFT Window Length</th>
<th>Hop Length</th>
<th>Resulting Input Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>S</td>
<td>20</td>
<td>4096</td>
<td>512</td>
<td>259 $\times$ 38</td>
</tr>
<tr>
<td>M</td>
<td>13</td>
<td>2048</td>
<td>256</td>
<td>517 $\times$ 24</td>
</tr>
<tr>
<td>L</td>
<td>7</td>
<td>1024</td>
<td>128</td>
<td>1034 $\times$ 12</td>
</tr>
</tbody>
</table>
Model  Since instrument classification is a more complex task than the synthetic workload in Section 4.1, a GRU [16] (described in Equations 4.3) is used in this set of experiments.

\[
\begin{align*}
\vec{R}_t &= W_{ir}\vec{x}_t + \vec{b}_{ir} + W_{hr}\vec{h}_{t-1} + \vec{b}_{hr} \\
\vec{r}_t &= \sigma(\vec{R}_t) \\
\vec{Z}_t &= W_{iz}\vec{x}_t + \vec{b}_{iz} + W_{hz}\vec{h}_{t-1} + \vec{b}_{hz} \\
\vec{z}_t &= \sigma(\vec{Z}_t) \\
\vec{M}_t &= W_{mn}\vec{h}_{t-1} + \vec{b}_{hn} \\
\vec{N}_t &= W_{m}\vec{x}_t + \vec{b}_{in} + \vec{r}_t \odot \vec{M}_t \\
\vec{n}_t &= \tanh(\vec{N}_t) \\
\vec{h}_t &= (1 - \vec{z}_t) \odot \vec{n}_t + \vec{z}_t \odot \vec{h}_{t-1} \\
\end{align*}
\]

(4.3)

where \( \vec{h}_t \in \mathbb{R}^{20} \), \( t \in \{0, \ldots, \text{frames} - 1\} \) and \( \vec{x}_t \in \mathbb{R}^{\text{coefficients}} \). Given the GRU expressed in the above form, the transposed Jacobian between consecutive hidden states \( \frac{\partial \vec{h}_t}{\partial \vec{h}_{t-1}} \) can be computed analytically:

\[
\begin{align*}
J_1 &= (\frac{\partial \vec{R}_t}{\partial \vec{h}_{t-1}})^T = W_{hr}^T, \quad J_2 = \text{Diag}(\frac{\partial \vec{r}_t}{\partial \vec{R}_t})^T = \vec{r}_t \circ (1 - \vec{r}_t) \\
J_3 &= \text{Diag}(\frac{\partial \vec{N}_t}{\partial \vec{M}_t})^T = \vec{M}_t, \quad J_4 = (\frac{\partial \vec{M}_t}{\partial \vec{h}_{t-1}})^T = W_{hn}^T \\
J_5 &= \text{Diag}(\frac{\partial \vec{N}_t}{\partial \vec{M}_t})^T = \vec{r}_t, \quad J_6 = \text{Diag}(\frac{\partial \vec{n}_t}{\partial \vec{N}_t})^T = 1 - \vec{n}_t \circ \vec{n}_t \\
J_7 &= \text{Diag}(\frac{\partial \vec{Z}_t}{\partial \vec{M}_t})^T = 1 - \vec{z}_t, \quad J_8 = (\frac{\partial \vec{Z}_t}{\partial \vec{h}_{t-1}})^T = W_{hz}^T \\
J_9 &= \text{Diag}(\frac{\partial \vec{Z}_t}{\partial \vec{M}_t})^T = \vec{z}_t \circ (1 - \vec{z}_t), \quad J_{10} = \text{Diag}(\frac{\partial \vec{h}_t}{\partial \vec{Z}_t})^T = \vec{h}_{t-1} - \vec{n}_t \\
J_{11} &= (\frac{\partial \vec{h}_t}{\partial \vec{h}_{t-1}})^T_{\text{direct}} = I \circ \vec{z} \\
\frac{\partial \vec{h}_t}{\partial \vec{h}_{t-1}} &= (J_1 \circ (J_2 \circ J_3)^T + J_4 \circ (J_5 \circ J_6)^T) \circ (J_6 \circ J_7)^T + J_8 \circ (J_9 \circ J_{10})^T + J_{11}
\end{align*}
\]

where \( \text{Diag}(\cdot) \) represents taking the diagonal of a square matrix, and \( \circ \) represents the broadcasting element-wise (Hadamard) product. Since cuDNN’s GRU implementation [3] is closed source, we cannot access the values of the gates (\( \vec{r}_t, \vec{z}_t, \vec{n}_t \)). Therefore, we have to recompute the gates (but in a more parallelized way) during the forward pass for computing \( \frac{\partial \vec{h}_t}{\partial \vec{h}_{t-1}} \) as shown in Equations 4.4. This engineering challenge results in significant overhead during the forward pass in our experiments, however, can potentially be resolved if cuDNN’s source code were publicly available. Other settings are the same as listed in Section 4.1.

Implementation  We use PyTorch’s GRU module [5] directly which calls into the cuDNN’s GRU implementations (\texttt{cudnn\textunderscore RNN\textunderscore Forward\textunderscore Training} and \texttt{cudnn\textunderscore RNN\textunderscore Backward\textunderscore Data} with \texttt{CUDNN\textunderscore GRU}) [40] to compete with the state-of-the-art baseline. We reuse the same CUDA implementation of the Blelloch scan algorithm as mentioned in Section 4.1.
4.3 Pruned VGG-11 Micro-benchmark

Despite the recent advances in network pruning algorithms [24, 56, 27], there is no existing widely adopted software or hardware platform that can exploit performance benefits from pruning, as most techniques are evaluated through “masking simulation” which leads to the same (if not worse) runtime and memory usage. In contrast, in this work, we discover that the retraining of pruned networks could benefit from BPPSA, since the values in the Jacobian of a convolution operator only depend on the filter weights based on Algorithm 4, and pruning the weights can lead to a higher sparsity in the Jacobian, which then reduces the per-step complexity of sparse matrix-matrix multiplications.

To evaluate the feasibility of leveraging the sparsity in the transposed Jacobian of each operator, we setup a benchmark on VGG-11 [58]: training on CIFAR-10 [33], pruning away 97% of the weights in all convolution and linear operators using the technique proposed by See et al. [56], and retraining the pruned network. We choose this pruning percentage so that a similar validation accuracy is reached (90.1% v.s. 88.9%) after retraining for the same number of epochs (100) as training. We then apply BPPSA on the convolutional layers of VGG-11 to compute Equation 2.3.

Since the sparsity pattern of the transposed Jacobian can be determined ahead of time from the model architecture (as we show in Section 3.3), the currently available sparse matrix libraries which target generic cases are sub-optimal for our method. For example, cuSPARSE [45] calculates the number of non-zeros in the product matrix and merges the indices of the input matrices before it can perform the multiplication. Such preparations do not need to repeat across iterations in BPPSA’s case and could be performed ahead of time due to the deterministic nature of the sparsity pattern. This, in turn, saves considerable amount of execution time. Therefore, due to the lack of a fair implementation, we perform our experiments by calculating the FLOPs needed for each step in our method and the baseline implementation through static analysis.
Chapter 5

Results

In this section, we present the results from the RNN end-to-end benchmark, the GRU end-to-end benchmark and the pruned VGG-11 micro-benchmark as described in Section 4.1, Section 4.2 and Section 4.3.

5.1 RNN End-to-end Benchmark with Synthetic Datasets

Figure 5.1 shows the training curves of loss values with respect to wall-clock time when we train the RNN for 50 epochs on the RTX 2070 GPU with the mini-batch size $B = 16$ and the sequence length $T = 1000$. This experiment can be viewed as the simplest mechanism to process sequential data such as audio signals. We observe that the blue curve (BPPSA) is roughly equivalent to the red curve (PyTorch/cuDNN baseline) scaled down by 54% along the horizontal axis. We conclude that, in this setting, training the RNN through BPPSA reconstructs the original back-propagation algorithm while achieving a 2.17× speedup on the overall training time and 4.53× on the BP runtime.

Sensitivity Analysis

We measure the performance variation as the sequence length $T$ and the batch size $B$ vary, since those two parameters represent the total number of operators $n$ and the number of (normalized) workers $p$ respectively — the key variables in the theoretical runtime of our method. To estimate the speedup on the overall training time, we measure the wall-clock time of training via BPPSA for a single epoch, and take the average of 10 measurements from different epochs. We then compare against training via the PyTorch/cuDNN baseline measured in the same way. We can also derive the speedup on only the backward pass by measuring the runtime of the training procedure without actually performing the backward pass, and subtracting from the total runtime (including the overhead of preparing the input transposed Jacobian matrices).

Figure 5.2a and Figure 5.2b show how changing the sequence length $T$ affects the backward pass and overall training time respectively. We make three observations from these two figures. First, our method scales as $n$ increases when $n$ is relatively in the same range as $p$. Second, when $n$ increases to be much larger than $p$, the performance starts to be bounded by $p$. Third, even in the range of overly large $n$, our method still achieves better utilization on massively parallel hardware than the baseline.

Figure 5.2c and Figure 5.2d show how changing the batch size $B$ affects the backward pass and overall training time respectively. We can conclude that BPPSA scales as the “effective” number of workers $p$...
Figure 5.1: Training loss across wall-clock time when the RNN is trained via BPPSA (blue curve) and the PyTorch Autograd baseline with cuDNN’s RNN backend (red curve).

(a) The speedup on the backward pass as the sequence length $T$ increases.

(b) The overall speedup as the sequence length $T$ increases.

(c) The speedup on the backward pass as the batch size $B$ decreases (equivalently, as the “effective” $p$ increases).

(d) The overall speedup as the batch size $B$ decreases (equivalently, as the “effective” $p$ increases).

Figure 5.2: The speedup in training of a single epoch (measured and averaged across 10 epochs) of our method against the baseline as the sequence length $T$ and the batch size $B$ varies. The blue and orange bars represent speedup on the RTX 2070 and 2080Ti GPUs. The red dash line represents the PyTorch Autograd [49] baseline with cuDNN’s RNN backend [3].
per sample increases (equivalently, as the batch size \( B \) decreases, since the total number of SMs in the GPU is constant). In reality, determining the appropriate mini-batch size can be nontrivial: training with large batch can lead to "generalization gap" \([31]\); while training with small batch would under-utilize the hardware resources and lead to longer training time. In this experiment, BPPSA can be viewed as offering an alternative to train with smaller mini-batch while utilizing the hardware resources more efficiently than BP.

By comparing the speedup in Figure 5.2a and Figure 5.2c between RTX 2070 and RTX 2080Ti, since RTX 2080Ti has a higher number of SMs than RTX 2070 (68 v.s. 36 \([48, 47]\)), we can observe that:
1) RTX 2080Ti achieves its maximum speedup at a higher sequence length compared with RTX 2070;
2) as the batch size \( B \) increases, the speedup of BPPSA on RTX 2080Ti drops at a slower rate than RTX 2070. These two observations are consistent with the aforementioned conclusions regarding the performance variation with the number of workers \( p \). The maximum backward pass and overall speedup can be observed from RTX 2080Ti, which are 2.75× and 8.8× respectively.

5.2 GRU End-to-end Benchmark with IRMAS

Figure 5.3 shows the training curves of loss values with respect to wall-clock time when we train the GRU with the \((S, M, L)\) preprocessed datasets for 400 epochs on the RTX 2070 GPU when the mini-batch size \( B \) is 16. We observe that the blue curve (BPPSA), if horizontally-scaled, maintains a similar shape as the red curve (PyTorch/cuDNN baseline), which reinforces our observation in Section 5.1 that BPPSA reconstructs the original back-propagation algorithm but achieves a shorter training time.

Sensitivity Analysis  To perform an analysis similar to Section 5.2, we only need to vary the batch size \( B \) since the preprocessed dataset type \((S, M, L)\) already reflects the sequence length \( T \). However, since the overhead of computing the transposed Jacobians during the forward pass cannot be neglected as mentioned in Section 4.2 to achieve a deeper understanding of the performance variation, we demonstrate the runtime breakdown among the forward pass, the backward pass and the overhead instead of only estimating the coarse-grained speedup. We can derive the overhead by measuring the runtime of the training procedure without actually performing the backward pass for both BPPSA and the PyTorch/cuDNN baseline, then taking the difference between them.

Figure 5.4 shows how the sequence length \( T \) and batch size \( B \) effect the runtime of the forward pass, the backward pass and the overhead. We make two observations from this figure. First, our method achieves a higher speedup on the backward pass as \( T \) increases (changing the dataset from \( S \) to \( L \)), which reinforces the observation from Section 5.1 that our method scales as the total number of operators \( n \) increases. Second, since the maximum sequence length (1034) is not as extreme as in Section 5.1, the backward pass runtime in BPPSA is relatively less affected by \( B \) and the GPU model than the overhead, which means \( n \) is still within the same range as the number of workers \( p \) in this set of experiments. Such overhead can be potentially resolved if we were able to modified the cuDNN’s GRU implementation. In this case, the maximum overall speedup and the backward pass speedup (excluding the overhead) are 2.11× and 13.45× respectively.
Chapter 5. Results

Figure 5.3: Training loss across wall-clock time when the GRU is trained via BPPSA (blue curve) and the PyTorch Autograd baseline with cuDNN’s RNN backend (red curve).

Figure 5.4: The runtime breakdown in training of a single epoch (measured and averaged across 400 epochs) of our method against the baseline for the \((S, M, L)\) datasets and different batch sizes \(B\). \(FP\) represents the runtime of the forward pass; \(FO\) represents the overhead of computing the transposed Jacobians during the forward pass; \(BP\) represents the runtime of the BP baseline; and \(BPPSA\) represents the backward pass runtime using our method. The measurements are normalized by the total runtime of the baseline \((FP + BP)\).
Figure 5.5: Measuring FLOP for each step when retraining pruned VGG-11 on CIFAR-10. The orange and blue circles represent matrix-vector and matrix-matrix multiplications in BPPSA respectively. A filled circle indicates that the step is on the critical path. The x-axis represents the theoretical runtime complexity of the step if the transposed Jacobian were not encoded in a sparse format. The green circles represent the FLOP estimated for each “gradient operator” in the baseline of the original BP.

5.3 Pruned VGG-11 Micro-benchmark

Since the sparsity of the product matrix might reduce after each multiplication, the per-step complexity might increase as the up-sweep phase progresses into deeper levels. Fortunately, we can adopt BPPSA to balance the number of levels in the up-/down-sweep phases according to the sparsity of the products on each level to achieve an overall speedup. Specifically, in this experiment, BPPSA performs the up-sweep phase from L0 to L2 (consistent with the notations in Figure 3.1), calculates the partial results that are needed for the down-sweep phase through linear scan, and then performs the down-sweep phase from L7 to L10.

Assuming the sparse transposed Jacobian matrices are encoded in the CSR format, Figure 5.5 shows the calculated FLOP of each step in BPPSA and each “gradient operator” in the baseline (BP) for re-training pruned VGG-11 on CIFAR-10. We can observe that the green circles (baseline) have similar expected performance as the other circles (BPPSA). Thus, we can conclude that exploiting the sparsity in the transposed Jacobian is an efficient strategy that reduces the per-step complexity of our method $P_{Blelloch}$ to a level similar with the baseline $P_{Linear}$. This strategy makes the overall scalability to be “guaranteed” algorithmically.
Chapter 6

Conclusion

In this work, we explore a novel direction to scale BP by challenging its fundamental limitation of the strong sequential dependency. We reformulate BP into a scan operation which is scaled by our modified version of the Blelloch scan algorithm. Our proposed algorithm, BPPSA, achieves a logarithmic runtime complexity rather than linear. In addition, BPPSA has a constant per-device space complexity; hence, its scalability is not limited by the memory capacity of each device. In our detailed evaluations, we demonstrate that overall speedup can be already achieved in two important use cases. First, for the case where there is a long dependency in BP, we evaluate BPPSA on two different sets of benchmarks: (1) training a RNN with synthetic datasets where our method achieves up to $2.75 \times$ speedup on the overall (end-to-end) training time and $8.8 \times$ speedup on the backward pass alone; and (2) training a GRU with the IRMAS dataset [11] where our method achieves up to $2.11 \times$ overall speedup and $13.45 \times$ speedup on the backward pass alone. Second, we can reduce the per-step complexity by leveraging the sparsity in the Jacobian itself. To this end, we develop efficient routines to generate the transposed Jacobian in the CSR format, and demonstrate that the retraining of pruned networks can potentially benefit from BPPSA (as we show for a pruned VGG-11 benchmark when re-training on the CIFAR-10 dataset). We hope that our work will inspire radically new ideas and designs to improve distributed DNN training beyond the existing theoretical framework.
Bibliography


